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LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106 LEGAL
MILPITAS, CA 95035

EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2181	3

DATE MAILED: 11/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/834,013	BESMER ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 is rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,313,588 to Nagashige et al. ("Nagashige").

In reference to Claim 1, Nagashige teaches a processor for forming a plurality of commands (analogous to the bus operation information structures of Claim 1) (See Figure 4 and Column 8 Lines 20-23); a command FIFO memory for storing the commands (See Figure 4 and Column 8 Lines 20-23); and a sequencer for processing the commands to perform the bus operations (See Figure 4 and Column 8 Lines 26-28); sequentially forming commands by the processor in the command FIFO memory (See Figure 4 and Column 8 Lines 20-23); storing the commands in the command FIFO memory (analogous to setting control over the bus operation information structure to the sequencer of Claim 1, since the memory is FIFO) (See Figure 4 and Column 8 Lines 20-20); the sequencer inherently checking the command FIFO memory to determine if a first command is present (analogous to determining if the sequencer has control over

the first bus operation information structure in the memory of Claim 1); the sequencer processing the first command upon determining that it has control over said first command (See Figure 4 and Column 8 Lines 26-28); the sequencer inherently checking the command FIFO memory to determine if a second command is present (analogous to determining if the sequencer has control over the second bus operation information structure in the memory of Claim 1); and the sequencer processing the second command upon determining that it has control over said second command (See Figure 4 and Column 8 Lines 36-40);

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 3, 5, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige as applied to Claim 1 above, and further in view of US Patent Number 6,205,506 to Richardson.

In reference to Claim 2, Nagashige teaches the limitations as applied to Claim 1 above. Nagashige does not teach a queue of pointers wherein each pointer is set to identify one of the bus operation information structures when the identified bus

operation information structure is ready for processing; placing a pointer identifying the first bus operation information structure in the queue of pointers by the processor upon forming the first bus operation information structure; and reading the pointer identifying the first bus operation information structure from the queue of pointers by the sequencer before processing the first bus operation information structure. Richardson teaches placing pointers to entries in a transaction buffer (analogous to the bus operation information structures of Claim 2) in a queue of pointers by the processor upon creation of said entries, which is also when they are ready for processing (See Column 5 Lines 10-19 of Richardson); and the bus interface unit (analogous to the sequencer of Claim 2) reading the pointer identifying the first entry in the transaction buffer from the queue of pointers before processing the first entry (See Column 5 Lines 19-25 of Richardson). Richardson further teaches the processor connected to the bus interface unit by a cache (See Column 5 Lines 64-67 of Richardson), said cache passing requests to the bus interface unit if it cannot service the request (See Column 1 Lines 22-34 of Richardson).

In reference to Claim 3, Nagashige teaches the limitations as applied to Claim 2 above. Nagashige further does not teach setting control over each bus operation information structure to the sequencer by placing the pointer identifying each bus operation information structure in the queue of pointers. Richardson further teaches that the pointer queues are first-in-first-out (See Column 6 Lines 45-49 of Richardson); that the pointers in the request queue point to entries which are to be transferred from the transaction buffer to the bus (See Column 6 Lines 66-67 and Column 7 Lines 1-10

of Richardson); and that the pointer queues are part of the bus interface unit (See Column 6 Lines 40-45 of Richardson). Therefore, the entries in the requesting queue are inherently controlled by the processor upon the pointer to said entry being placed in the request queue.

In reference to Claim 5, Nagashige and Richardson teach the limitations as applied to Claim 2 above. Nagashige further does not teach the queue of pointers being a first queue of pointers and the system further comprising a second queue of pointers wherein each pointer is set to identify one of the bus operation information structures when the identified bus operation information structure has been processed; placing a pointer identifying the first bus operation information structure in the second queue of pointers by the sequencer after processing the first bus operation information structure; reading the pointer identifying the first bus operation information structure from the second queue of pointers by the processor; and forming a third bus operation information structure in the same memory space containing the first bus operation information structure. Richardson further teaches multiple pointer queues (See Column 5 Lines 10-13 and Column 6 Lines 40-51 of Richardson) wherein each pointer is set to identify one of the transaction requests when said request has been processed (See Column 7 Lines 29-31 of Richardson); that a pointer to a transaction that has been completed on the bus can be placed in a completion status queue (analogous to the second queue of pointers of Claim 5) (See Column 7 Lines 24-31 of Richardson); transferring the pointer from the completion status queue to the cache which transfers it to the processor (See Column 7 Lines 32-36 of Richardson); and marking the entry in

the transaction buffer corresponding to said pointer as empty (See Column 7 Lines 36-39 of Richardson) which allows a new transaction request (analogous to the bus operation information structure of Claim 5) to be loaded into that space in the transaction buffer (See Column 6 Lines 55-58 of Richardson).

In reference to Claim 6, Nagashige teaches the limitations as applied to Claim 1 above. Nagashige does not teach a queue of pointers wherein each pointer is set to identify one of the bus operation information structures when the identified bus operation information structure has been processed; placing a pointer identifying the first bus operation information structure in the queue of pointers by the sequencer after processing the first bus operation information structure; reading the pointer identifying the first bus operation information structure from the queue of pointers by the processor; and forming a third bus operation information structure in the same memory space containing the first bus operation information structure. Richardson teaches a queue of pointers wherein each pointer is set to identify one of the transaction requests when said request has been processed (See Column 5 Lines 10-13 and Column 7 Lines 29-31 of Richardson); that a pointer to a transaction that has been completed on the bus can be placed in a completion status queue (See Column 7 Lines 24-31 of Richardson); transferring the pointer from the completion status queue to the cache which transfers it to the processor (See Column 7 Lines 32-36 of Richardson); and marking the entry in the transaction buffer corresponding to said pointer as empty (See Column 7 Lines 36-39 of Richardson) which allows a new transaction request to be loaded into that space in the transaction buffer (See Column 6 Lines 55-58 of Richardson). Richardson further

teaches the processor connected to the bus interface unit by a cache (See Column 5 Lines 64-67 of Richardson), said cache passing requests to the bus interface unit if it cannot service the request (See Column 1 Lines 22-34 of Richardson).

In reference to Claim 7, Nagashige and Richardson teach the limitations as applied to Claim 6 above. Nagashige further does not teach setting control over each bus operation information structure to the processor by placing the pointer identifying each bus operation information structure in the queue of pointers. Richardson teaches that the pointer queues are first-in-first-out (See Column 6 Lines 45-49 of Richardson) and that the pointers in the completion status queue point to entries which are to be transferred from the transaction buffer to the processor (See Column 7 Lines 24-36 of Richardson). Therefore, the entries in the completion status queue are inherently controlled by the processor upon the pointer to said entry being placed in the completion status queue.

One of ordinary skill in the art at the time the invention was made would combine the device of Nagashige with the device of Richardson, resulting in the invention of Claim 2, 3, 5, 6, and 7, in order to allow different classes of information to be stored separately as well as to maintain ordering information for each entry in the transaction buffer (See Abstract, Column 5 Lines 19-22, Column 6 Lines 40-45, and Column 8 Lines 15-18 of Richardson).

5. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige and Richardson as applied to Claims 2 and 7 above, and further in view of US Patent Number 6,047,339 to Su et al. ("Su").

In reference to Claim 4, Nagashige and Richardson teach the limitations as applied to Claim 2 above. Nagashige and Richardson do not teach the queue of pointers supplying a start flag to the sequencer whenever the queue of pointers contains a pointer that has not been read by the sequencer; asserting the start flag after placing the pointer identifying the first bus operation information structure in the queue of pointers; and determining that the sequencer has control over the first bus operation information structure by receiving the start flag by the sequencer and reading the pointer identifying the first bus operation information structure from the queue of pointers. Su teaches sending a signal to a read controller (analogous to the sequencer of Claim 4) indicating that unread data is present in the memory bank (analogous to the queue of pointers of Claim 4) (See Column 4 Lines 37-40 and Column 5 Lines 33-61 of Su); asserting the start flag upon placing data in a memory bank (See Column 5 Lines 33-34 of Su); and the read controller determining that the data in the memory bank can be read by receiving the start flag and reading the data from the memory bank (analogous to determining that the sequencer has control over the first bus operation information structure of Claim 4) (See Column 5 Lines 46-56 of Su)

In reference to Claim 8, Nagashige and Richardson teach the limitations as applied to Claim 7 above. Nagashige and Richardson further do not teach the queue of pointers supplying a complete flag to the processor whenever the queue of pointers

contains a pointer that has not been read by the processor; asserting the complete flag after placing the pointer identifying the first bus operation information structure in the queue of pointers; and determining that the processor has control over the first bus operation information structure by receiving the complete flag by the processor and reading the pointer identifying the first bus operation information structure from the queue of pointers. Su teaches sending a signal to a read controller (analogous to the processor of Claim 8) indicating that unread data is present in the memory bank (analogous to the queue of pointers of Claim 8) (See Column 4 Lines 37-40 and Column 5 Lines 33-61 of Su); asserting the start flag (analogous to the complete flag of Claim 8) upon placing data in a memory bank (See Column 5 Lines 33-34 of Su); and the read controller determining that the data in the memory bank can be read by receiving the start flag and reading the data from the memory bank (See Column 5 Lines 46-56 of Su).

One of ordinary skill in the art at the time the invention was made would combine the device of Nagashige and Richardson with the device of Su, resulting in the invention of Claims 4 and 8, in order to allow the processor to communicate with a sequencer operating at a different speed (See Column 1 Lines 12-28 of Su).

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige as applied to Claim 1 above, and further in view of US Patent Number 6,434,650 to Morris et al. ("Morris").

In reference to Claim 9, Nagashige teaches the limitations as applied to Claim 1 above. Nagashige does not teach sending a signal from the processor to the sequencer to start processing the first bus operation information structure upon forming said first bus operation information structure. Morris teaches a transmitter (analogous to the processor of Claim 9) driving a control signal low when it is ready to transmit data to the co-processor (analogous to signaling the sequencer to begin processing, of Claim 9) (See Figures 1, 1a, and 3, and Column 8 Lines 6-12 of Morris).

One of ordinary skill in the art at the time the invention was made would combine the device of Nagashige with the device of Morris, resulting in the invention of Claim 9, in order to provide a means of flow control (See Column 6 Lines 63-67 of Morris).

7. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige and Morris as applied to Claim 9 above, and further in view of US Patent Number 5,726,985 to Daniel et al. ("Daniel").

In reference to Claim 10, Nagashige and Morris teach the limitations as applied to Claim 9 above. Nagashige and Morris do not teach associating the bus operation information structure with a link to the next bus operation information structure upon forming each bus operation information structure; and after processing each bus operation information structure by the sequencer, determining which bus operation information structure is to be processed next by reading the associated link to the next bus operation information structure. Daniel teaches a FIFO memory in which each element (analogous to the bus operation information structure of Claim 10) contains a

link to the next element, said link being maintained by the scheduler (analogous to the processor of Claim 10), said maintenance inherently being performed upon adding an element to the linked-list FIFO (See Column 15 Lines 45-57 of Daniel); and the APU (analogous to the sequencer of Claim 10) determining which element to transmit next based on the link information of the current element, since they are transmitted in FIFO order and each element contains a link to the next element (See Column 29 Lines 35-39 of Daniel).

In reference to Claim 11, Nagashige, Morris, and Daniel teach the limitations as applied to Claim 10 above. Nagashige and Morris further do not teach each bus operation information structure including a link field which indicates the next bus operation information structure; and setting the link field of the bus operation information structure to the next bus operation information structure to associate the bus operation information structure wit the link. Daniel teaches that the link information is contained in a link field of the element (See Figure 7 and Column 15 Lines 40-47 of Daniel); and the link field being maintained by the scheduler (analogous to the processor of Claim 26), said maintenance inherently being performed upon adding an element to the linked-list FIFO (See Column 15 Lines 45-57 of Daniel).

One of ordinary skill in the art at the time the invention was made would combine the device of Nagashige, Su, and Kang with the device of Daniel, resulting in the inventions of Claims 25 and 26, in order to allow elements to be inserted into the middle of the FIFO structure without disturbing and reordering the remainder of the list (See Column 7 Lines 47-56 of Daniel).

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige and Morris as applied to Claim 9 above, and further in view of Su.

In reference to Claim 12, Nagashige and Morris teach the limitations as applied to Claim 9 above. Nagashige and Morris do not teach each bus operation information structure including an owner field that indicates whether the processor or the sequencer has control over the bus operation information structure; setting the owner field to the sequencer by the processor to set control over the bus operation information structure to the sequencer upon forming each bus operation information structure; and setting the owner field to the processor by the sequencer after processing each bus operation information structure. Su teaches a plurality of memory banks (analogous to the bus operation information structures of Claim 12) that each includes a status flag that can be used to indicate ownership of the corresponding bank (See Column 4 Lines 30-32, Column 5 Lines 38-39, and Column 5 Lines 52-54 of Su); the write controller (analogous to the processor of Claim 12) setting the status flag to a value of "start" (analogous to setting the owner field to the sequencer of Claim 12) upon writing data to the memory bank (analogous to forming a bus operation information structure of Claim 12) (See Column 5 Lines 33-34 of Su); and the read controller (analogous to the sequencer of Claim 12) setting the status flag to a value of "done" (analogous to setting the owner field to the processor of Claim 12) after reading the data in the memory bank (See Column 5 Lines 49-56 of Su).

In reference to Claim 13, Nagashige and Morris teach the limitations as in Claim 9 above. Nagashige and Morris do not teach setting control over the bus operation information structure to the processor before forming the bus operation information structure; determining whether the sequencer or the processor has control over the second bus operation information structure after processing the first bus operation information structure; and waiting for the processor to send a signal to the sequencer to start processing the second bus operation information structure upon determining that the processor has control over the second bus operation information structure. Su inherently teaches that each memory bank status flag is initially set to a value of "done", since a memory location cannot be read from before it is written to; and thereafter, every write operation will be preceded by a read operation, which sets the value of the status flag to "done" (analogous to setting control over the bus operation information structure before forming each bus operation information structure of Claim 13). Su further teaches the read controller (analogous to the sequencer of Claim 13) determining if the value of the status flag for the second memory bank is "start" (analogous to determining if the processor has control over the second bus operation information structure of Claim 13) after reading the first memory bank (analogous to processing the first bus operation information structure of Claim 13) (See Column 5 Lines 49-51 of Su); and waiting until the write controller (analogous to the processor of Claim 13) sets the value of the status flag to "start", indicating that the read controller now has control of the memory bank (See Column 5 Lines 51-56 of Su);

One of ordinary skill in the art at the time the invention was made would combine the device of Nagashige and Morris with the device of Su, resulting in the inventions of Claims 12 and 13, in order to allow the processor to communicate with a sequencer operating at a different speed (See Column 1 Lines 12-28 of Su).

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige and Morris as applied to Claim 9 above, and further in view of US Patent Number 6,263,445 to Blumenau.

In reference to Claim 11, Nagashige and Morris teach the limitations as applied to Claim 9 above. Nagashige further teaches that the bus adapter includes the sequencer and the memory spaces (See Figure 4 and Column 7 Lines 51-58 of Nagashige). Nagashige and Morris do not teach the computer system including a CPU and a bus adapter; the bus adapter including the processor; sending a plurality of I/O messages from the CPU to the bus adapter; receiving the I/O messages at the processor in the bus adapter; and forming the bus operation information structures from the I/O messages. Blumenau teaches a computer system that has a CPU (See Figure 3 and Column 6 Lines 28-33 of Blumenau) and a bus adapter that includes a processor and memory (See Figure 3 and Column 6 Lines 46-51 of Blumenau); the CPU sending data (analogous to the I/O messages of Claim 14) to the bus adapter (See Column 6 Lines 36-38 of Blumenau); the processor in the bus adapter receiving data (See Column 6 Lines 36-38 and Column 6 Lines 47-49 of Blumenau); and forming packets (analogous to the bus operation information structures of Claim 14) compatible with the

network protocol from the data received from the CPU (See Column 6 Lines 36-38 and Column 6 Lines 51-53 of Blumenau).

One of ordinary skill in the art at the time the invention was made would combine the device of Nagashige and Morris with the device of Blumenau, resulting in the invention of Claim 14, in order to provide a means to connect the host processor to the bus (See Column 6 Lines 35-36 of Blumenau) and to convert the data received from the CPU into a format compatible with the bus (See Column 6 Lines 36-38 of Blumenau).

10. Claims 15, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige in view of Su.

In reference to Claim 15, Nagashige teaches a bus (See Figure 4 and Column 7 Lines 51-58 of Nagashige); a command FIFO memory for storing the commands (analogous to the bus operation information structures) (See Figure 4 and Column 8 Lines 20-23 of Nagashige); a sequencer connected to the memory and the bus to perform the bus operations on the bus upon processing the commands (See Figure 4 and Column 7 Lines 51-58 of Nagashige); a processor connected to the memory spaces and the sequencer to sequentially form the commands in the memory spaces (See Figure 4 and Column 8 Lines 20-23 of Nagashige); the sequencer processing the first command upon determining that it has control over said first command (See Figure 4 and Column 8 Lines 26-28 of Nagashige); and the sequencer processing the second command upon determining that it has control over said second command (See Figure 4 and Column 8 Lines 36-40 of Nagashige). Nagashige does not teach a plurality of

control indicators indicating control status over the bus operation information structures; said control indicators connected to the sequencer to indicate that the sequencer has control over the bus operation information structure; said control indicators further connected to the processor and generated by the processor causing the sequencer to process the formed bus operation information structures; and the sequencer processing a first one of the bus operation information structures upon receiving a first one of the control indicators and the sequencer processing a second one of the bus operation information structures upon completion of processing the first bus operation information structure if a second one of the control indicators indicates that the sequencer has control over the second bus operation information structure. Su teaches status flags (analogous to the control indicators of Claim 15) for memory banks (analogous to the bus operation information structures of Claim 15) (See Column 2 Lines 26-33 of Su); a read controller (analogous to the sequencer of Claim 15) connected to the status flags that reads the data in the memory bank (analogous to performing the bus operation described by the bus operation information structure of Claim 15) if the status flag has a value of "start" (analogous to indicating the sequencer has control of Claim 15) (See Column 5 Lines 46-47 of Su); a write controller (analogous to the processor of Claim 15) connected to the status flags that sequentially writes data to the memory banks (analogous to forming the bus operation information structures of Claim 15) and sets the status flag to the value of "start" (See Column 5 Lines 33-38 of Su); the read controller reading the data in the first memory bank when the first status flag has a value of "start" (See Column 5 Lines 46-47 of Su); and the sequencer reading the second memory

bank upon completion of reading the first memory bank if the second status flag has a value of "start" (See Column 5 Lines 46-56 of Su).

In reference to Claim 18, Nagashige and Su teach the limits as applied to Claim 15 above. Su further teaches the write controller writing data to the memory (analogous to forming the second bus operation information structure of Claim 18) upon completion of writing the first memory bank if there is a memory bank available (See Column 5 Lines 33-45 of Su). Nagashige and Su do not teach the control indicators including a queue of pointers wherein each pointer is set to identify one of the bus operation information structures when the identified bus operation information structure has been processed by the sequencer and the memory space containing the processed bus operation information structure is available for a new bus operation information structure to be formed therein; the sequencer sending the pointers to the queue of pointers identifying the available memory spaces in the order that the bus operation information structures contained therein were processed after processing the bus operation information structures; the processor reading the pointers from the queue of pointers in the order in which the pointers were sent to the queue of pointers and forming the next bus operation information structure in one of the available memory spaces; and the processor proceeding to form the second bus operation information structure if there is at least the one available memory space upon completing forming the first bus operation information structure. Richardson teaches a queue of pointers wherein each pointer identifies a transaction that has completed processing and the buffer space of said transaction is available (See Column 7 Lines 30-40 of Richardson); the queue of

pointers from the sequencer identifying the available memory spaces being a FIFO queue (analogous to sending the pointers to the queue of pointers in the order that they were processed of Claim 18) (See Column 6 Lines 40-52 of Richardson); a pointer being acted on when it reaches the head of a FIFO queue (analogous to the processor reading the pointers from the queue of pointers in the order in which the pointers were sent to the queue of pointers of Claim 18) (See Column 7 Lines 33-37 of Richardson).

In reference to Claim 19, Nagashige and Su teach the limitations as applied to Claim 18 above. Su further teaches sending a signal to a write controller (analogous to the processor of Claim 19) indicating that there is a location in the memory bank (analogous to the queue of pointers of Claim 19) that has not been acted on by the write controller (See Column 4 Lines 37-40 and Column 5 Lines 33-61 of Su); and writing data to the next memory bank (analogous to forming the next bus operation information structure) upon completing writing data to the previous memory bank if there is an available memory bank and upon receiving the done flag (analogous to the complete flag of Claim 19) if none of the memory banks are currently available (See Column 5 Lines 33-42 of Su).

One of ordinary skill in the art at the time the invention was made would combine the device of Nagashige with the device of Su, resulting in the inventions of Claims 15, 18, and 19, in order to allow the processor to communicate with a sequencer operating at a different speed (See Column 1 Lines 12-28 of Su).

11. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige and Su as applied to Claim 15 above, and further in view of Richardson.

In reference to Claim 16, Nagashige and Su teach the limitations as applied to Claim 15 above. Nagashige and Su do not teach the control indicators including a queue of pointers, each pointer being set to identify one of the bus operation information structures when the identified bus operation information structure is ready for processing; the processor sending the pointers to the queue of pointers identifying the formed bus operation information structures in the order that the bus operation information structures were formed after forming the bus operation information structures; the sequencer reading the pointers from the queue of pointers in the order in which the pointers were sent to the queue of pointers and processes the bus operation information structures in the same order; and the sequencer proceeding to process the second bus operation information structure if the queue of pointers contains a pointer for the second bus operation information structure. Richardson teaches placing pointers to entries in a transaction buffer (analogous to the bus operation information structures of Claim 16) in a queue of pointers by the processor upon creation of said entries, which is also when they are ready for processing (See Column 5 Lines 10-19 of Richardson); placing a pointer to a newly created transaction entry in the queue of pointers upon creation of said entry (See Column 6 Lines 58-61 of Richardson); the bus interface unit (analogous to the sequencer of Claim 16) reading a pointer from the head of the FIFO queue of pointers (See Column 7 Lines 6-10 of Richardson); and

processing the next transaction entry pointed to by the pointer at the head of the queue of pointers upon completion of processing the first transaction entry (See Column 7 Lines 17-23 of Richardson). Richardson further teaches the processor connected to the bus interface unit by a cache (See Column 5 Lines 64-67 of Richardson), said cache passing requests to the bus interface unit if it cannot service the request (See Column 1 Lines 22-34 of Richardson).

In reference to Claim 17, Nagashige, Su, and Richardson teach the limitations as applied to Claim 16 above. Nagashige further teaches setting a command presence indicator (analogous to the start flag of Claim 17) that indicates the presence of a command in the command queue that hasn't been processed by the sequencer (See Abstract and Column 8 Lines 23-26 of Nagashige); and the sequencer processing the next command in the command queue upon completing processing the previous command if the command presence indicator is set and upon the command presence indicator being set if no command is currently being processed by the sequencer (See Abstract and Column 8 Lines 26-42 of Nagashige).

One of ordinary skill in the art at the time the invention was made would combine the device of Nagashige and Su with the device of Richardson, resulting in the inventions of Claims 16 and 17, in order to allow different classes of information to be stored separately as well as to maintain ordering information for each entry in the transaction buffer (See Abstract, Column 5 Lines 19-22, Column 6 Lines 40-45, and Column 8 Lines 15-18 of Richardson).

12. Claims 20, 22, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige and Su as applied to Claim 15 above, and further in view of US Patent Number 6,052,133 to Kang.

In reference to Claim 20, Nagashige and Su teach the limitations as applied to Claim 15 above. Su further teaches that the status flags can be stored in the memory device (analogous to each bus operation information structure including the control information indicating control status of Claim 20) (See Column 4 Lines 30-32 of Su). Nagashige and Su do not teach the sequencer performing the bus operation described by each bus operation information structure if the sequencer receives a start signal; the processor sending the start signal to the sequencer to start processing the first bus operation information structure; and the sequencer processing the first bus operation information structure upon receiving the start signal. Kang teaches a PCI bridge/cache controller unit (analogous to the processor of Claim 20) that sends a start signal to a unified graphics/video controller (analogous to the sequencer of Claim 20) followed by a command and corresponding address and data information (analogous to the bus operation information structure of Claim 20) (See Figure 6, Column 6 Lines 66-67, and Column 7 Lines 1-19 of Kang).

In reference to Claim 22, Nagashige, Su, and Kang teach the limitations as applied to Claim 20 above. Su further teaches the write controller setting the status flag for a memory bank to a value of "start" (analogous to indicating that the sequencer has control over the bus operation information structure of Claim 22) upon writing data to the memory bank (See Column 5 Lines 33-34 of Su); and the read controller setting the

status flag for a memory bank to a value of "done" (analogous to indicating that the processor has control over the bus operation information structure of Claim 22) upon reading the data in the memory bank (See Column 5 Lines 47-49 of Su).

In reference to Claim 23, Nagashige, Su, and Kang teach the limitations as applied to Claim 20 above. Su further teaches that the read controller does not read the data from a memory bank if the status flag does not have a value of "start" (analogous to indicating that the sequencer has control over the bus operation information structure of Claim 23) (See Column 5 Lines 49-56 of Su). Nagashige and Su further do not teach the sequencer waiting to receive the start signal from the processor before processing the second bus operation information structure. Kang further teaches that the graphics/video controller waits to receive the start signal before beginning to perform the task specified by the command (See Column 7 Lines 5-14 of Kang).

In reference to Claim 24, Nagashige, Su, and Kang teach the limitations as applied to Claim 20 above. Su further teaches that each memory bank can include a status flag that also indicates ownership (See Column 4 Lines 30-32, Column 5 Lines 38-39, and Column 5 Lines 52-54 of Su); and the status flag being set by the write controller (analogous to the processor of Claim 24) after writing data to the memory bank (analogous to forming the bus operation information structure) to indicate that the data has been written and may be read by the read controller (analogous to the sequencer of Claim 24).

One of ordinary skill in the art at the time the invention was made would combine the device of Nagashige and Su with the device of Kang, resulting in the invention of

Claims 20, 22, 23, and 24, in order to produce a more efficient device since the sequencer will only receive commands from one place (See Column 2 Lines 37-41 of Kang).

13. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige, Su, and Kang as applied to Claim 20 above, and further in view of Blumenau.

In reference to Claim 21, Nagashige, Su, and Kang teach the limitations as applied to Claim 20 above. Nagashige further teaches that the bus adapter includes the sequencer and the memory spaces (See Figure 4 and Column 7 Lines 51-58 of Nagashige). Nagashige, Su, and Kang do not teach the bus adapter including a processor; the processor being operative to form the bus operation information structures from received I/O messages; a CPU connected to the bus adapter at the processor and operative according to software programming to prepare the I/O messages to the bus adapter; and the I/O messages defining I/O operations to be performed through the bus. Blumenau teaches a computer system that has a CPU (See Figure 3 and Column 6 Lines 28-33 of Blumenau) and a bus adapter that includes a processor and memory (See Figure 3 and Column 6 Lines 46-51 of Blumenau); the processor in the bus adapter receiving data (analogous to the I/O messages of Claim 21) (See Column 6 Lines 36-38 and Column 6 Lines 47-49 of Blumenau) and forming packets (analogous to the bus operation information structures of Claim 21) compatible with the network protocol from the data received from the CPU (See Column 6 Lines 36-

38 and Column 6 Lines 51-53 of Blumenau); and the data defining the I/O operations to be performed through the bus (See Column 6 Lines 36-38 of Blumenau). The CPU of Blumenau would inherently be responsive to software programming to prepare the data and to send the data to the bus adapter.

One of ordinary skill in the art at the time the invention was made would combine the device of Nagashige, Su, and Kang with the device of Blumenau, resulting in the invention of Claim 21, in order to provide a means to connect the host processor to the bus (See Column 6 Lines 35-36 of Blumenau) and to convert the data received from the CPU into a format compatible with the bus (See Column 6 Lines 36-38 of Blumenau).

14. Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige, Su, and Kang as applied to Claim 20 above, and further in view of Daniel.

In reference to Claim 25, Nagashige, Su, and Kang teach the limitations as applied to Claim 20 above. Su further teaches the read controller (analogous to the sequencer of Claim 25) checking the status flag (analogous to the control information of Claim 25) to determine if it should begin reading the data in the memory bank (analogous to the bus operation information structure of Claim 25) (See Column 5 Lines 49-56 of Su). Nagashige, Su, and Kang do not teach each bus operation information structure including link information indicating a next one of the bus operation information structures to be processed by the sequencer after processing a current one of the bus operation information structures to be processed by the sequencer after processing a

current one of the bus operation information structures; and the sequencer determining which one of the bus operation information structures is the next bus operation information structure from the link information of the current bus operation information structure and determining whether to begin processing the next bus operation information structure from the control information of the next bus operation information structure. Daniel teaches a FIFO memory in which each element (analogous to the bus operation information structure of Claim 25) contains a link to the next element to be transmitted (analogous to processed by the sequencer of Claim 25) after transmitting the current element (See Figures 3 and 4, Column 7 Lines 44-46, and Column 29 Lines 24-39 of Daniel); and the APU (analogous to the sequencer of Claim 25) determining which element to transmit next based on the link information of the current element, since they are transmitted in FIFO order and each element contains a link to the next element (See Column 29 Lines 35-39 of Daniel).

In reference to Claim 26, Nagashige, Su, Kang, and Daniel teach the limitations as applied to Claim 25 above. Nagashige, Su, and Kang do not teach each bus operation information structure including a link field containing the link information; and the link field of each bus operation information structure being set by the processor to indicate the next bus operation information structure upon forming the current bus operation information structure. Daniel teaches that the link information is contained in a link field of the element (See Figure 7 and Column 15 Lines 40-47 of Daniel); and the link field being maintained by the scheduler (analogous to the processor of Claim 26),

said maintenance inherently being performed upon adding an element to the linked-list FIFO (See Column 15 Lines 45-57 of Daniel).

One of ordinary skill in the art at the time the invention was made would combine the device of Nagashige, Su, and Kang with the device of Daniel, resulting in the inventions of Claims 25 and 26, in order to allow elements to be inserted into the middle of the FIFO structure without disturbing and reordering the remainder of the list (See Column 7 Lines 47-56 of Daniel).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (8-5:30), Alt. Fridays (8-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-5631.

tjc

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Thomas J. Cleary
Patent Examiner
Art Unit 2181